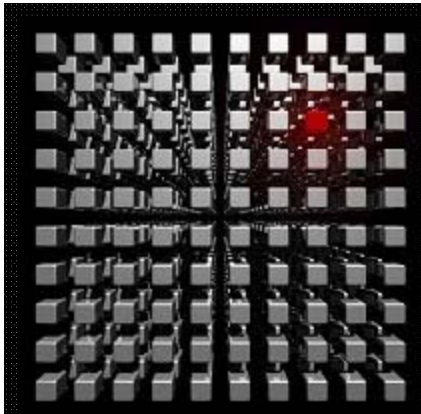

Inventing the Future of Computing

Parallella: A $99 Open Hardware Parallel Computing Platform

Andreas Olofsson
andreas@adapteva.com

IPDPS
May 22th, Cambridge, MA

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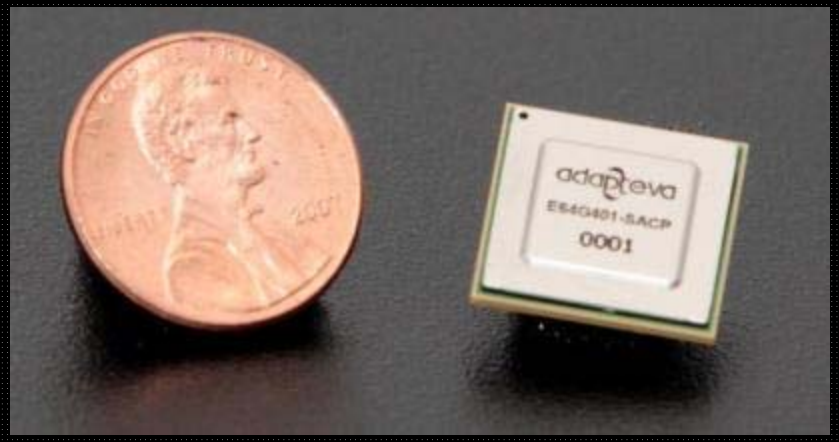
Adapteva Achieves 3 "World Firsts"

1. First commercial processor to reach 50 GFLOPS/W



2. First mobile processor with an open source OpenCL™ SDK

3. First semiconductor company to successfully crowd-source project

KICKSTARTER

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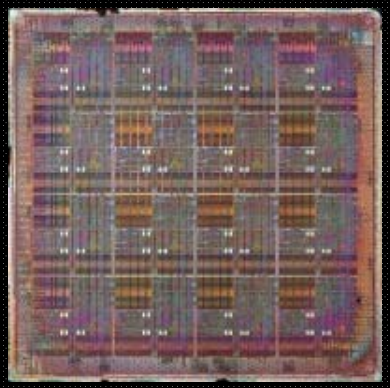
Adapteva's Goals in 2008

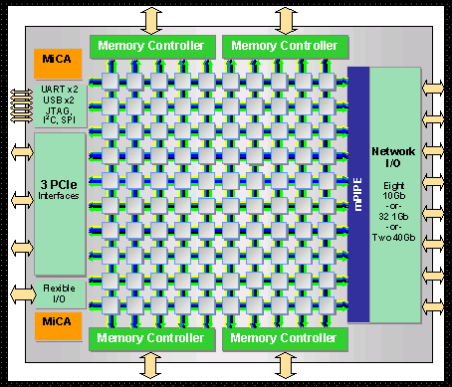
- A C/C++ programmable multicore processor
- Scalable to 1000's of cores on a chip
- Native IEEE floating point support
- Easy to Use
- 50 GFLOPS/Watt in 65nm

Our Inspiration

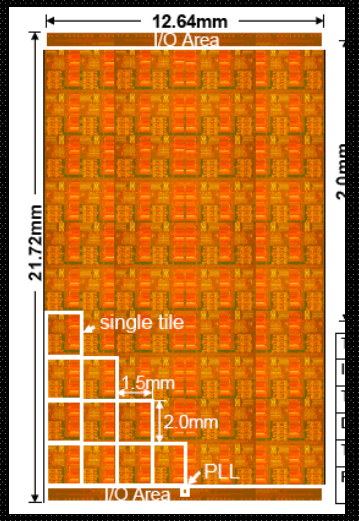
Transputer
Inmos
(1984)



RAW
MIT
(1997)



Tile
Tilera
(2006)



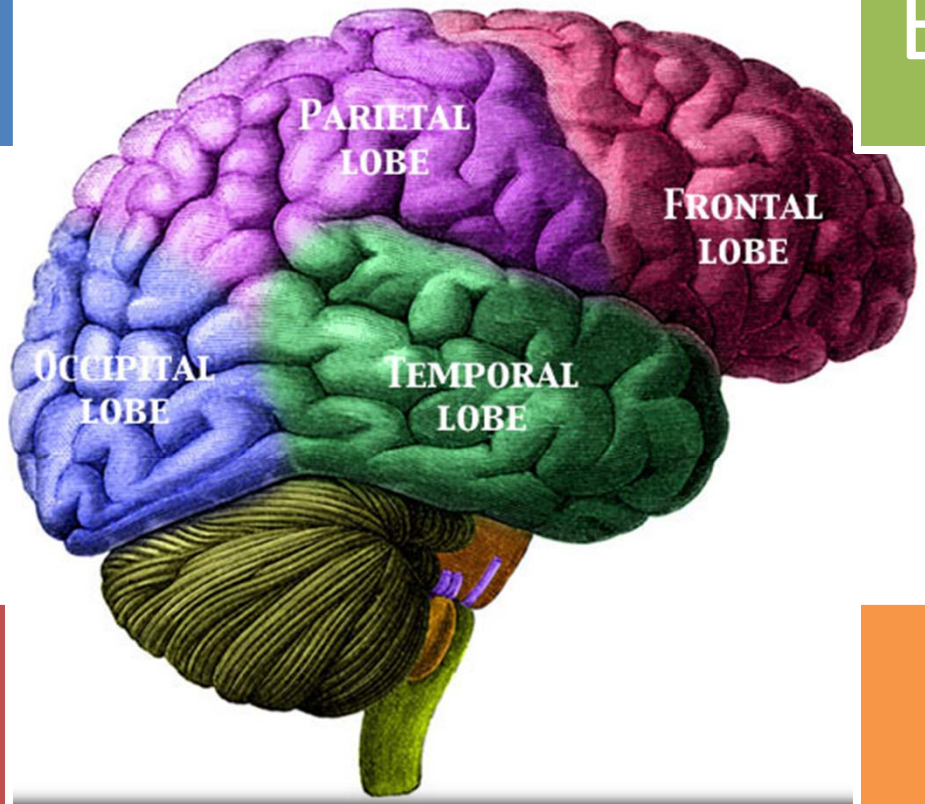
Teraflop
Intel
(2007)

http://www.adapteva.com/white-papers/the-siren-song-of-parallel-computing/

Our guiding light

Parallel

Efficient



Hetero-geneous

Robust

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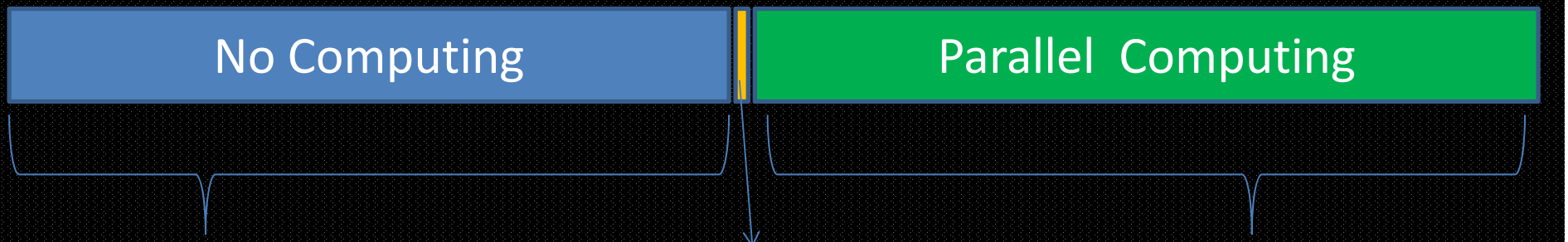
Any Reason to Think the Future of Computing is NOT Parallel?



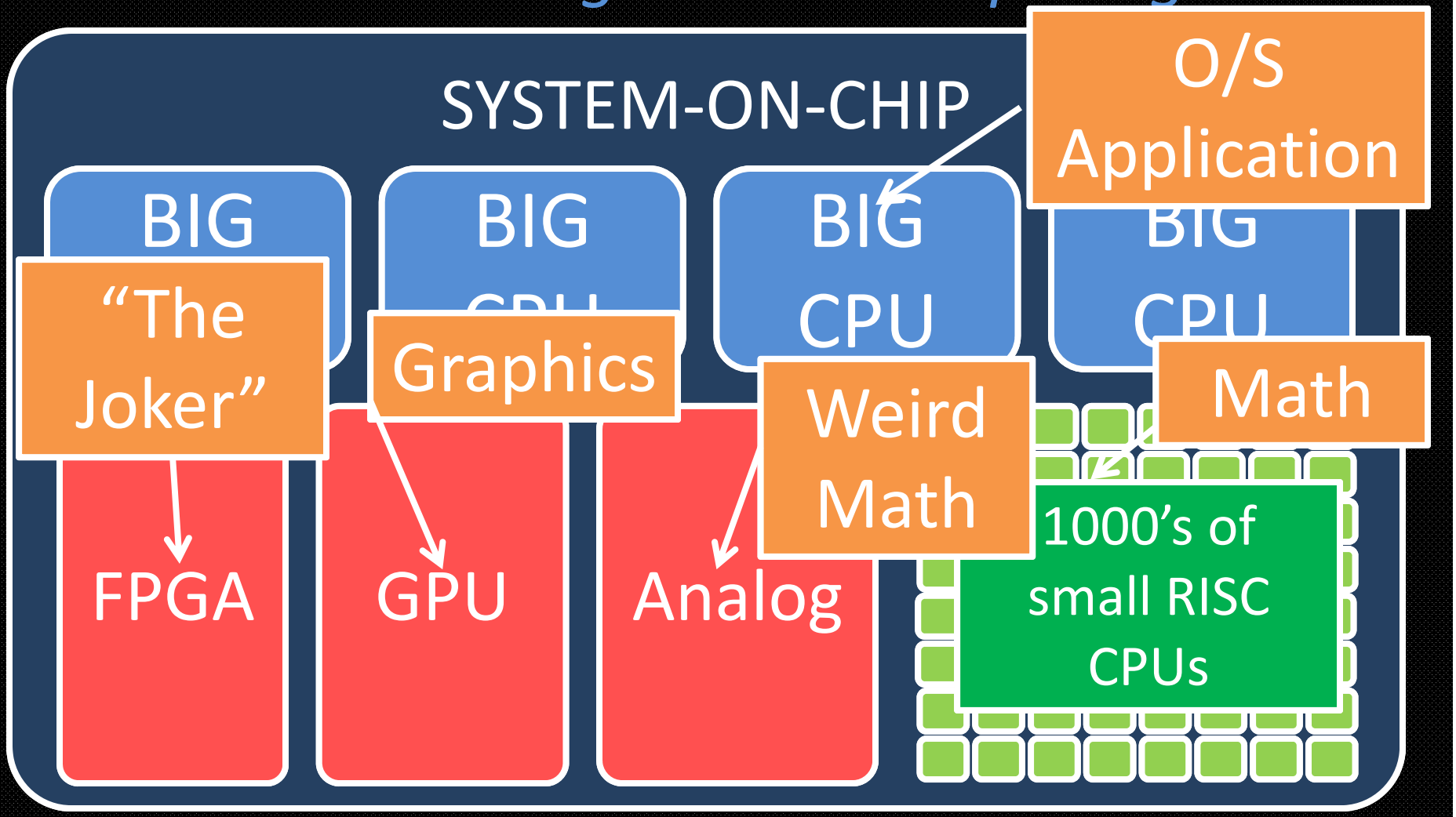
No Electronic Computing -1943

"Von Neumann Age" Serial Computing 1943-2013?

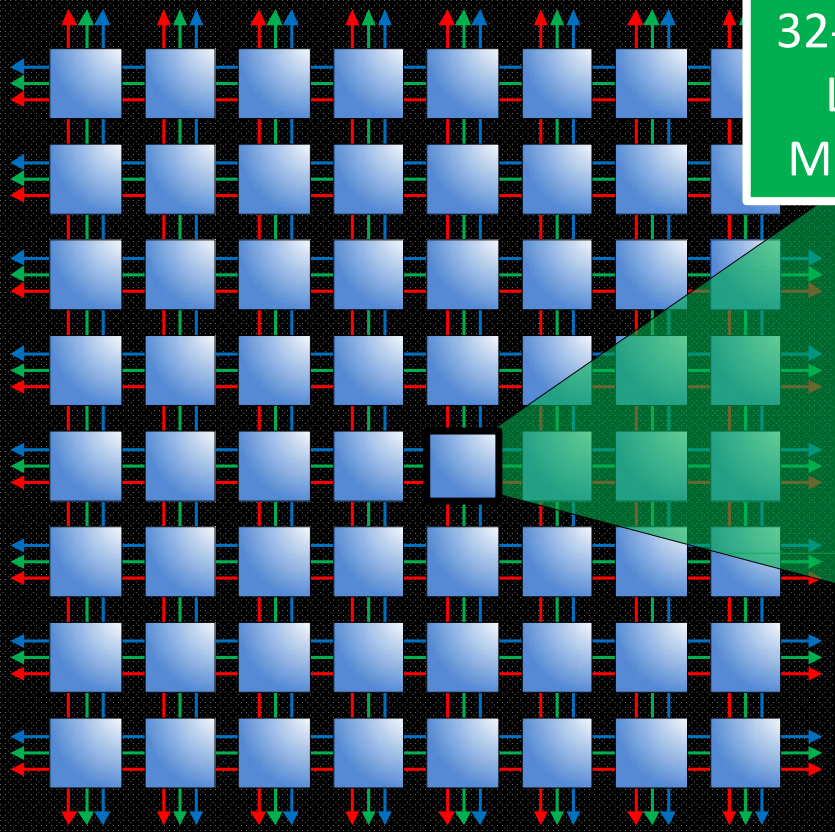
Parallel Computing 2013-??

A Practical Start:

True Heterogeneous Computing



The Epiphany Coprocessor



32-128KB Local Memory

1 GHz RISC Core

Local Memory

Multicore Framework

1.6 GFLOPS Per Core @ ~25mW

Router

Packet Based Network-On-Chip With 100GB/s Bisection BW

Coprocessor for ARM/x86 Host

<20pJ / FLOP !

MIMD/Task-Parallel Accelerator

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Pragmatic Architecture Tradeoffs

IN

- Dual issue RISC processors
- 64 entry register file
- Shared memory architecture
- 32-128KB per core memory
- Multi-banked local memory
- Packet based Mesh NOC
- 32 Bit IEEE float/int arithmetic
- Memory protection
- Timers, Interrupts, DMAs

OUT

- Any special purpose instructions
- Hardware caching
- SIMD
- Optimized remote read accesses
- Memory management unit
- Strict memory order model

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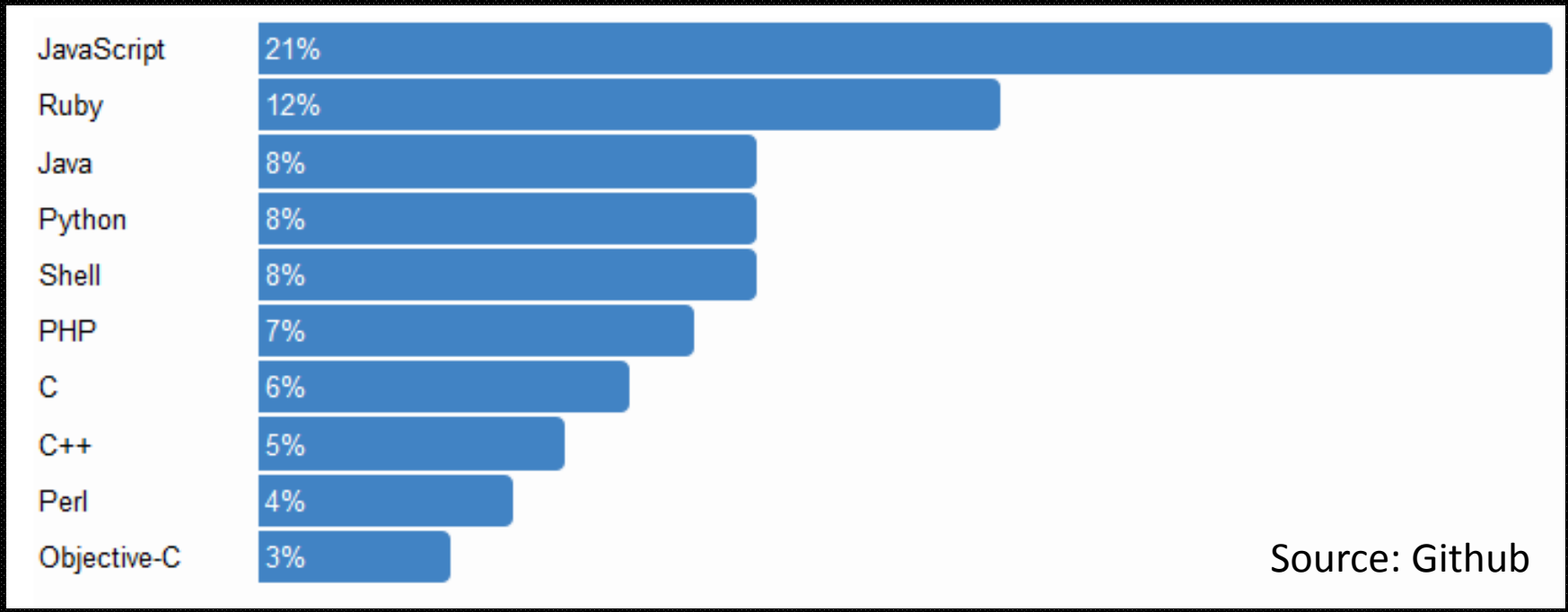
How the $#@% Do We Program This Thing?

The Current State of Parallel Programming



How To Make Every Programmer a Parallel Programmer?

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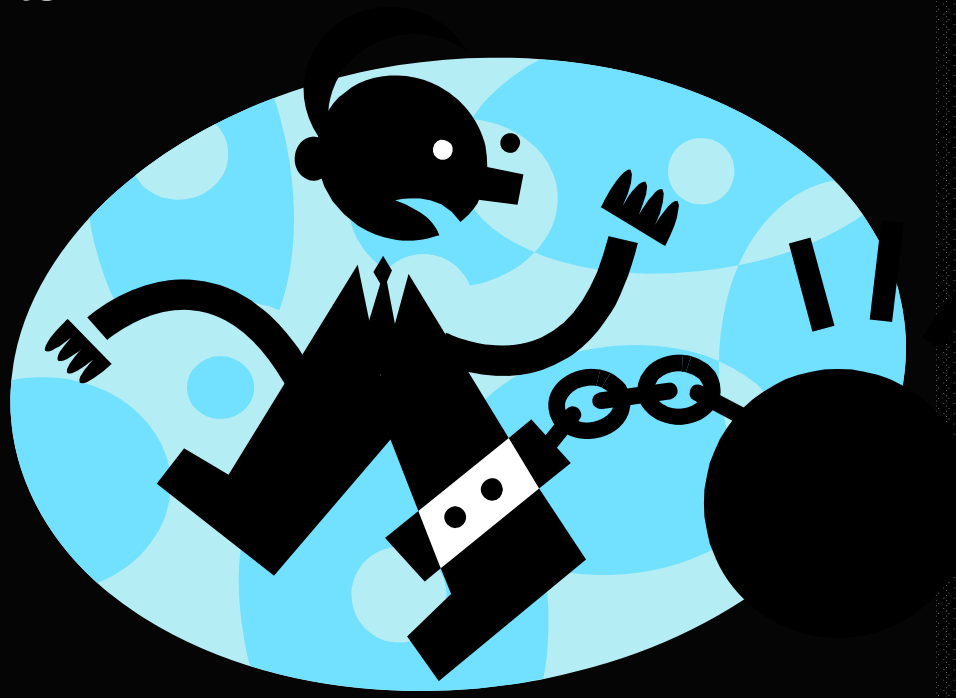
Parallel Programming Frameworks

Erlang	SystemC	Intel TBB	Co-Fortran	Lisp	Janus
Scala	Haskell	Pragmas	Fortress	Hadoop	Linda
Smalltalk	CUDA	Clojure	UPC	PVM	Alef
Julia	OpenCL	Go	X10	Posix	XC
Occam	OpenHMPP	ParaSail	APL	Simulink	Charm++
Occam-pi	OpenMP	Ada	Labview	Ptolemy	StreamIt
Verilog	OpenACC	C++ Amp	Rust	Sisal	Star-P
VHDL	Cilk	Chapel	MPI	MCAPI	?????????

Stupid Hurdles That Get in the Way of Progress

- Proprietary SDKs and programming frameworks
- Lack of datasheets/documents
- Closed source drivers
- Expensive lock-in hardware
- NDA requirements
- Exlcusive access



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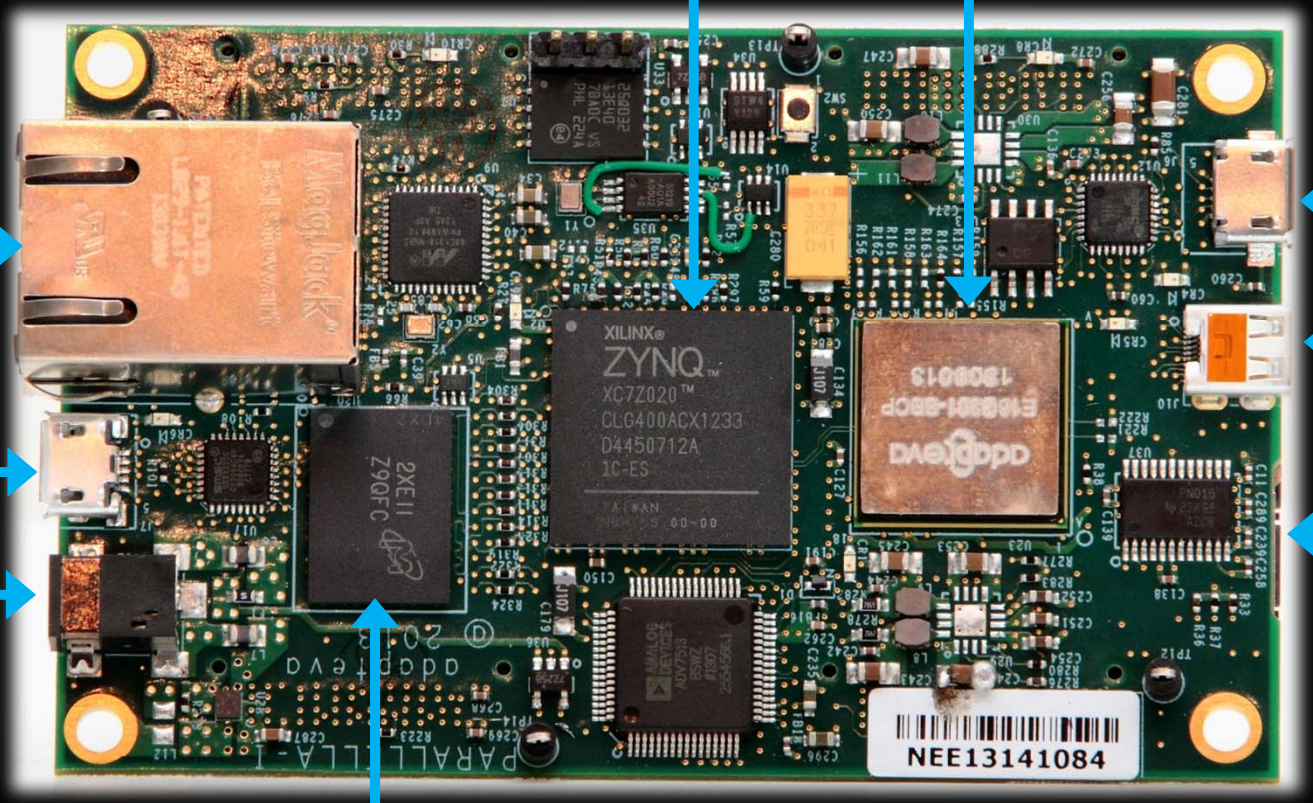
The Parallella Project Guidelines

- A $99 single board ”parallel” computer that runs Linux
- Open source (SDK, board files, drivers) (github.com/parallella)
- Open documentation (adapteva.com/all-documents)
- Open to all (forums.parallella.org)

The Parallella Board

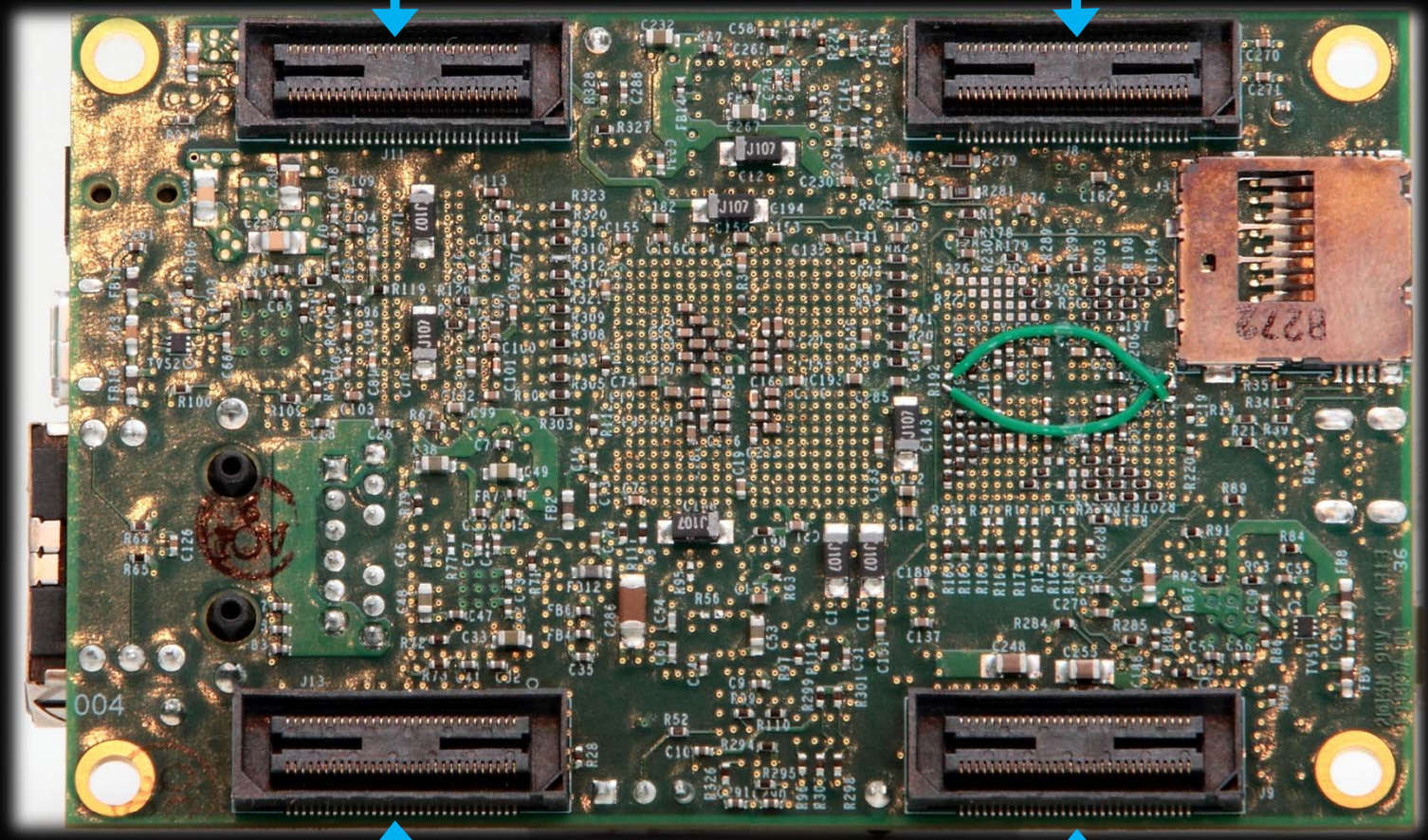


The Parallella Backside (optional)

6 GB/s ! BW

FPGA Logic Connector

Epiphany North Connector



Instrumentation Connector

Epiphany South Connector

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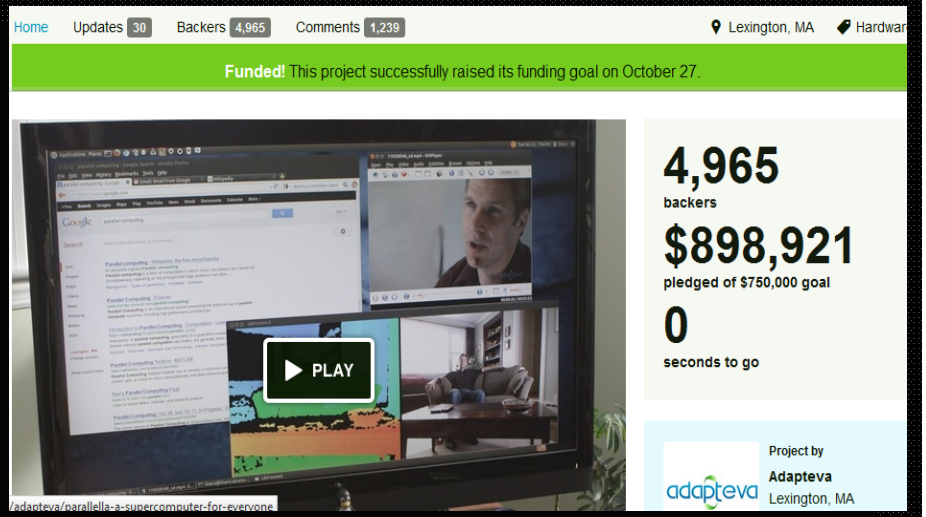
Parallella Kickstarter Campaign

- 5,000 customers
- 6,300 boards ”pre-sold” in 4 weeks
- 67 countries, all 50 US states
- 50-75% of backers are developers
- 11,000 more signups since Jan 1st



- Backer Application Interest:
  - Software Defined Radio
  - Ray tracing/rendering
  - Image processing
  - Robotics
  - Gaming
  - Cryptography
  - Parallel computing research
  - Distributed Computing
  - Machine Learning
  - HPC

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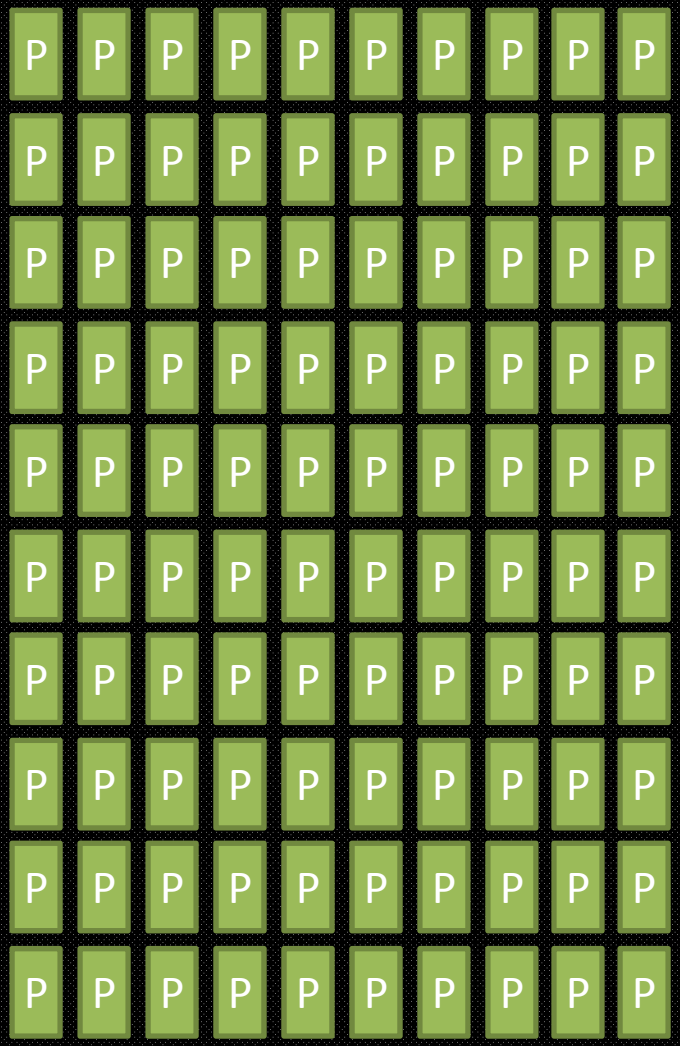
The Parallella 1% Academic Program



- Adapteva will donate (at least) 1 board for every 100 boards sold!
- Open to all academic institutions active in parallel computing research & education

Program starts June 1st, 2013!

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