A Scalable Processor Architecture for the Next Generation of Low Power Supercomputer

PRACE Workshop, October 2010
Andreas Olofsson
Company Introduction

• Company founded in 2008 with mission to produce programmable processors with 10x the energy efficient of existing products while using 1/10\textsuperscript{th} of the development budget

• Veteran processor design team with 10 successful low power products, 100M units shipped, and over $200M in product related revenue

• Adapteva has completed development of a ground breaking programmable soft accelerator with energy efficiency of up to 50 GFLOPS/Watt

• Now sampling first product to lead customers and strategic partners
Why efficient supercomputing is a critical need!

Data from James Anderson at Lincoln Labs and Top500

6x in 3 years
2.5x in 3 years
# DARPA UHPC Program

<table>
<thead>
<tr>
<th>System Element</th>
<th>Goals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cabinet</td>
<td>Cabinet: width &lt; 24 inches; height &lt; 78 inches; and depth &lt; 40 inches</td>
</tr>
<tr>
<td>Form Factor</td>
<td>50 GFLOPS/W LINPACK (HPL) benchmark</td>
</tr>
<tr>
<td>Energy Efficiency</td>
<td>1 PFLOPS (HPL)</td>
</tr>
<tr>
<td>Peak Performance</td>
<td>57 kW including: UHPC System, storage system, fans, self contained cooling, high bandwidth I/O, etc.</td>
</tr>
<tr>
<td>Maximum Cabinet Power</td>
<td>Self contained within cabinet. All approaches not requiring external resources are allowable.</td>
</tr>
<tr>
<td>Cooling</td>
<td>Support of massive streaming sensor data</td>
</tr>
<tr>
<td>Numeric Format – Floating Point</td>
<td>IEEE754 single and double precision, sufficient to support HPC compatible implementations of IEEE754</td>
</tr>
<tr>
<td>Numeric Format – Fixed Point</td>
<td>16, 32, and 64-bit supporting all arithmetic and</td>
</tr>
</tbody>
</table>

Big Winners: INTEL, NVIDIA, MIT, SANDIA
Bad News for Semi. Companies

IC Design Costs
(feature dimensions vs. cost. in $)
(millions)

Prototype
Validation
Physical
Verification
Architecture

Source: International Business Strategies
More Bad News..

- $10M development cost per chip
- ARM RISC Core up to 120MHz
- USB 2.0, Ethernet, CAN, GPIO, etc
- 512KB flash, 65KB SRAM
- 12 bit A/D, 10 bit D/A

$2.36 in 10ku

VS.

$4

- Coffee beans
- Water..
Area vs Max Performance (65nm)

What if we could borrow only the best features?

Ease of Use

Efficient CPU

Accelerator

Scale

AMD-OPTERON
36 GFLOPS
283 mm^2

IBM CELL
210 GFLOPS
220 mm^2

VIRTEX5-LX50
48 GMACS
146 mm^2

NVIDIA-GTX280
933 GFLOPS
576 mm^2
# A History of Embedded Processing

<table>
<thead>
<tr>
<th>PERIOD</th>
<th>“MAC-DSP” ERA</th>
<th>VLIW/SIMD ERA</th>
<th>FPGA ERA</th>
<th>“MANYCORE” ERA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1985-1995</td>
<td>ENERGY EFFICIENCY</td>
<td>ENERGY EFFICIENCY &amp; EASE OF USE</td>
<td>ENERGY EFFICIENCY &amp; FLEXIBILITY &amp; SCALABILITY</td>
<td>ENERGY EFFICIENCY &amp; SCALABILITY &amp; EASE OF USE</td>
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<tr>
<td>1995-2005</td>
<td>ENERGY EFFICIENCY</td>
<td>ENERGY EFFICIENCY &amp; EASE OF USE</td>
<td>ENERGY EFFICIENCY &amp; FLEXIBILITY &amp; SCALABILITY</td>
<td>ENERGY EFFICIENCY &amp; SCALABILITY &amp; EASE OF USE</td>
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<tr>
<td>2005-2015</td>
<td>ENERGY EFFICIENCY &amp; SCALABILITY</td>
<td>ENERGY EFFICIENCY &amp; FLEXIBILITY &amp; SCALABILITY</td>
<td>ENERGY EFFICIENCY &amp; SCALABILITY &amp; EASE OF USE</td>
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<tr>
<td>2015-</td>
<td>ENERGY EFFICIENCY &amp; SCALABILITY</td>
<td>ENERGY EFFICIENCY &amp; FLEXIBILITY &amp; SCALABILITY</td>
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</tbody>
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<table>
<thead>
<tr>
<th>ACHILLES HEEL(s)</th>
<th>PROGRAMMING MODEL</th>
<th>NOT SCALABLE</th>
<th>AREA INEFFICIENT</th>
<th>??</th>
</tr>
</thead>
<tbody>
<tr>
<td>NORMALIZED PERFORMANCE (GFLOP/W)</td>
<td>1-2</td>
<td>0.5-2</td>
<td>0.5-5</td>
<td>50</td>
</tr>
</tbody>
</table>

The future of embedded processing is programmable massively parallel multicore chips!
Epiphany™ Signal Processing Fabric

- Easy to use programming model
- Scalable to 1000's of cores
- IEEE Floating Point Compliant

- 25-50 GFLOP/W at 65nm
- 0.7mm per processing tile
- 100 GFLOP/W at 28nm
Architecture Summary

Memory Model:
- HW driven caches kill energy efficiency!
- Cache misses very expensive!
- So..NO HW caches.
- Distributed Flat Shared Memory
- All memory accessible by all cores
- 32KB multi bank SRAM per core

Network- On-Chip:
- Wires are cheap!
- 104 bit atomic packets
- One packet per clock cycle
- 1 ns per hop

CPU:
- Stability is expensive!
- Optimized for math
- “Good enough” for control code
- 1 GHz operation
- 2 FLOPS/cycle
- 64 entry register file
A Very Simple Flat Memory Model

- Completely unprotected
- Examples of core to core communication:
  - STR R0, [R1,#42]
  - LDR R0, [R1,#42]
Network On Chip Routing Algorithm

- Each processor node has x,y coordinate
- Destination address compared to mesh node address to determine direction
- Reads are “write requests”
- X-first, then Y
# Architecture Comparison

<table>
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<tr>
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</thead>
<tbody>
<tr>
<td><strong>Process</strong></td>
<td>65nm</td>
<td>90nm</td>
<td>45nm</td>
<td>45nm</td>
<td>65nm</td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
<td>3.13GHz</td>
<td>850MHz</td>
<td>2GHz</td>
<td>648MHz</td>
<td>500MHz</td>
</tr>
<tr>
<td><strong>Cores</strong></td>
<td>80</td>
<td>64</td>
<td>48</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td><strong>Area (mm^2)</strong></td>
<td>275</td>
<td>n/a</td>
<td>567</td>
<td>16</td>
<td>12</td>
</tr>
<tr>
<td><strong>Transistors (Million)</strong></td>
<td>100</td>
<td>615</td>
<td>1300</td>
<td>n/a</td>
<td>40</td>
</tr>
<tr>
<td><strong>Performance (GLFOPS)</strong></td>
<td>1000</td>
<td>No Native Floating Point</td>
<td>n/a</td>
<td>36</td>
<td>16</td>
</tr>
<tr>
<td><strong>Power (W)</strong></td>
<td>200</td>
<td>10</td>
<td>125</td>
<td>0.85</td>
<td>0.35</td>
</tr>
<tr>
<td><strong>Area/Core(mm)</strong></td>
<td>3.43</td>
<td>n/a</td>
<td>11.81</td>
<td>2</td>
<td>0.72</td>
</tr>
<tr>
<td><strong>Watt/ (GHZ*Cores)</strong></td>
<td>0.8</td>
<td>0.18</td>
<td>1.3</td>
<td>0.16</td>
<td>0.04</td>
</tr>
</tbody>
</table>
A “Programmer's Architecture”

- “Task-Channel” Programming Model
- ANSI-C Programmable using efficient GNU C-compiler
- Runs floating point C-programs out of the box!
- No special program constructs needed!
- Native single cycle floating point instruction support!
- Shared memory architecture
- Orthogonal register and instruction set
Robust Programming Environment

MULTICORE PROGRAMMING MODEL/LIBS
(IN DEVELOPMENT)

ECLIPSE IDE
(AVAILABLE)

GNU COMPILER
(AVAILABLE)

WYSIWYG SIMULATOR
(AVAILABLE)

GNU DEBUGGER
(AVAILABLE)

GNU BINUTILS
(AVAILABLE)
**FFT Mapping Example**

- **Approach:**
  - 1024 point FFT is spread over 16 processors
  - $s_1,s_2,s_3,s_4$ refer to the four FFT stages for combining data with 64 point complex data movements
  - Lower # procs transfer $W_0$ to higher # procs.
  - Lower # proc calculates $W_{j0} + W_{j1} \times C_j$, higher # proc calculates $W_{j0} - W_{j1} \times C_j$

- **Results:**
  - <3us execution time
  - High efficiency
  - Work in progress, still room for improvement
Compromised Computing

What users want:
An easy to use C programmable device with infinite energy, zero power consumption, and all interconnect standards

Soft Floating Point Accelerator

The compromise:
- Microprocessor takes care of the really complex stuff
- FPGA driven connectivity
- A soft accelerator takes care of the “10% code”
A Radar Signal Chain Example

- A/D
  - Mult-channel
  - High Data Rate

- FRONT-END (ASIC/FPGA)
  - 10,000+ Giga-ops
  - Filterering
  - Fixed Point
  - Low Complexity

- NEW! MIDDLE-END
  - 1000-10,000 Gigaflop
  - Adaptive Beamforming
  - Pulse Compression
  - Floating Point
  - Medium Complexity

- BACK-END (uP)
  - 10-100 Gigaflop
  - Clutter
  - Target Detection
  - Large Code
  - High Complexity

- • Implementing complex floating point algorithms in FPGA too complex
- • Microprocessor based middle end processing far too power hungry
- • The answer is a new device optimized for this type middle-end floating point signal processing!
**Arcitecture Application Sweet-spot**

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**What our customers want!**
- Floating point
- Massive performance
- Lower power (<3 W) per chip
- C-programmability and "ease of use"
- Scalability

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<table>
<thead>
<tr>
<th>GREAT FIT APPLICATIONS BASED ON CUSTOMER INTERVIEWS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Portable Ultrasound</td>
</tr>
<tr>
<td>Airborne Radar</td>
</tr>
<tr>
<td>Automotive Radar</td>
</tr>
<tr>
<td>Antenna Beam-forming</td>
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</tbody>
</table>
E16xx Product Intro (samples available!)

Features:
- 16 Independent Processor Cores
- 4 full duplex FPGA LVDS links
- 4Mb On-chip Shared Memory
- 65nm IBM Process Platform

Performance
- 350mW core power at 500MHz!
- 32 GFLOPS/sec max performance
- 8 GB/sec Off-chip Bandwidth
- 512 GB/sec On-chip Bandwidth

Availability:
- Silicon in lab confirms power advantage
- Currently sampling to lead customers
Short Term Product Roadmap

Q4 2010
- 16 CPUs
- 1GHz
- 32GFLOPS
- <2 Watt
- 65nm

Q3 2011
- 64 CPUs
- 1.5GHz
- 256 GFLOPS
- <2.5 Watt
- 28nm

SCALABLE
- >100 GFLOP/WATT

1024 CPUs
- 1.5GHz
- 4 TFLOPS
- <40 Watt
- 28nm

Performance

16 CPUs
- 1GHz
- 32GFLOPS
- <2 Watt
- 65nm
Development ECO System

- **State of the art Tool Chain: (available now!)**
  - Optimized GNU-C compiler
  - Multi-core debugger
  - Standard Eclipse IDE
  - Standard C and Math library
  - Unique guaranteed 100% accurate WYSIWYG chip simulator

- **Evaluation Boards: (available now!)**
  - Plugin boards for standard Altera FPGA development kits
  - FPGA emulation board available for SW/HW co-development

- **Software Libraries: (available November)**
  - Multi-core FFT implementation
  - Multi-core programming libraries
Adapteva HPC Capabilities

- Adapteva, Bittware, and Petapath brings together key expertise in chip, board, and software design enabling fast execution of prototype HPC systems.
  
- 64-128 GFLOP FMC (VITA 57) accelerator card available 3/15/11

- 1 TFLOP 50-Watt accelerator card in the works for Q2 2011

- Will continue to grow library support base on customer feedback

- Can spin double precision floating point chip with very limited funding
Adapteva Board Offering

- Based on Altera Stratix IV Family
- Attaches to ATCA carriers or other cards equipped with AMC bays and used in MicroTCA system
- Advanced FPGA framework simplifies system design.
- <50 Watts with daughter card
- Base card available today
- Daughter card available 3/15

FPGA handles back plane connectivity

FMC Connector enables up to 128 GFLOPS of soft performance with Adapteva chips.
A straw-man 1 TFLOP, 50 Watt AMC card

- 1 TFLOP of performance
- 16 MB of distributed memory
- X GB of on-board memory
- Shows off performance density achievable
- Probably not practical for any real applications
Conclusions

• The next generation supercomputers will not be practical without a radically different architecture

• The only way to improve energy efficiency significantly is through compromise

• Adapteva has developed a software programmable floating point accelerator demonstrating 25 GFLOPS/W in silicon and 100 GFLOPs/W on the road map for 2011

• The programming model needs to change..but not drastically
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