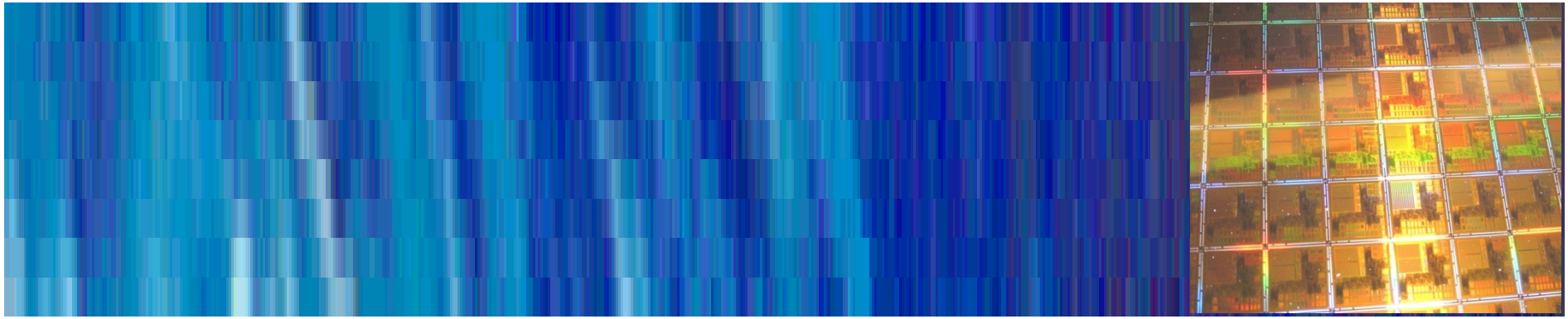
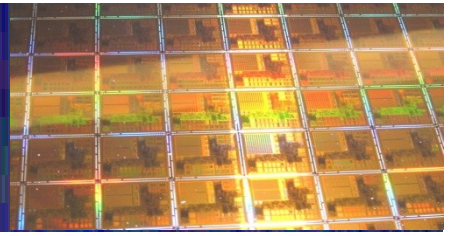


Peaceful coexistence among architectures

Andreas Olofsson, Adapteva
andreas@adapteva.com
HPEC 2009

ADAPTEVA

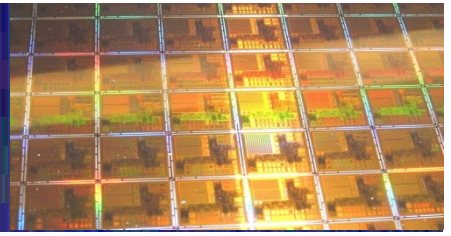
Introduction to Adapteva



- We are a fabless semiconductor company busy developing the world's most energy efficient C-programmable floating point processors targeted at embedded applications.

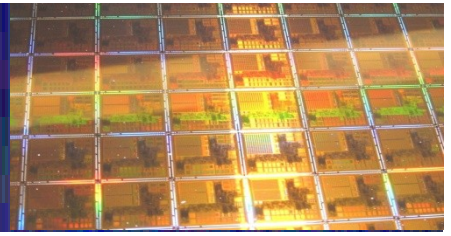
- Prototype in hand, product slated for middle of next year

Why ASICs?



- Because flexibility wastes energy:
  - Given the same conditions ASICs have a 50x-1000x energy efficiency edge over GPUs, DSPs, FPGAs, and Microprocessors.
- The problems:
  - Expensive to (re)design, long turnaround times
  - Very difficult to get specification right the first time
  - Limited number of design teams who can design deep sub-micron ASICs

Breaking down ASIC costs

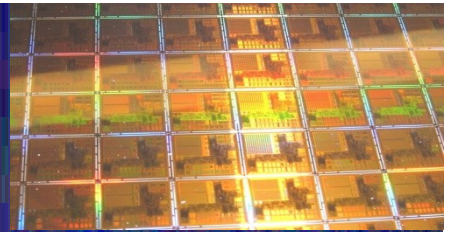


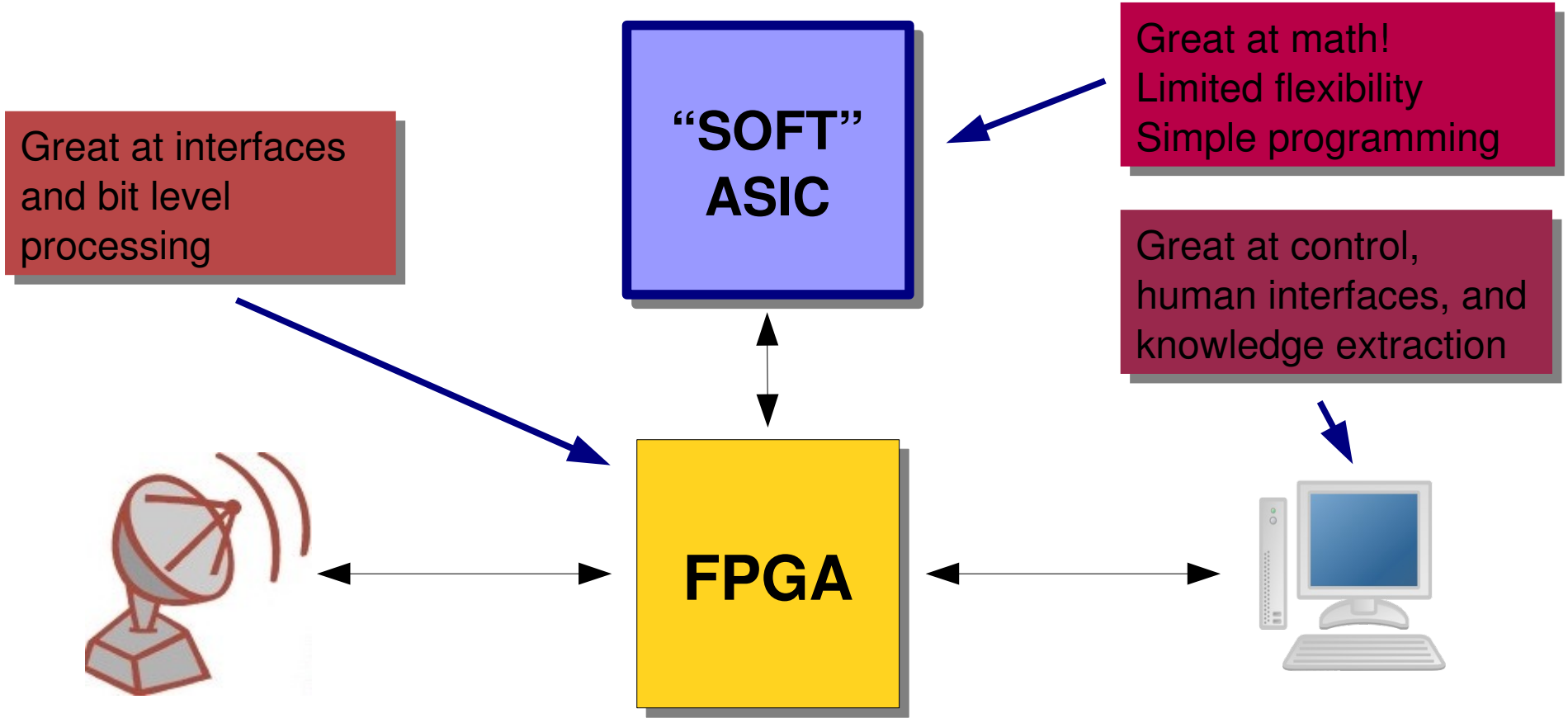
- "The cost of ASICs are sky rocketing", Moshe Gavrielov, CEO at Xilinx

	SOC	ASIC	FPGA
HARDWARE	$16,875,000	$1,200,000	$900,000
SOFTWARE	$6,750,000	$300,000	$300,000
TOOLS	$5,000,000	$500,000	$0
FABRICATION	$2,500,000	$200,000	$0
IP	$5,000,000	$500,000	$0
TOTAL	$36,125,000	$2,700,000	$1,200,000

- Conclusion: Architecture development cost is heavily dependent on architecture and end application

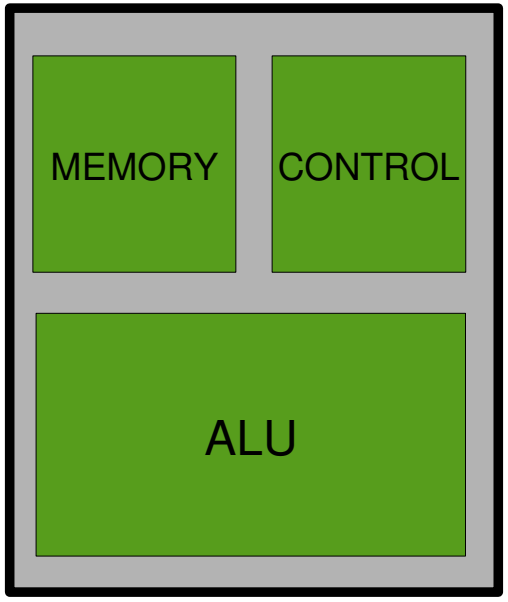
The "Ideal" Embedded Solution



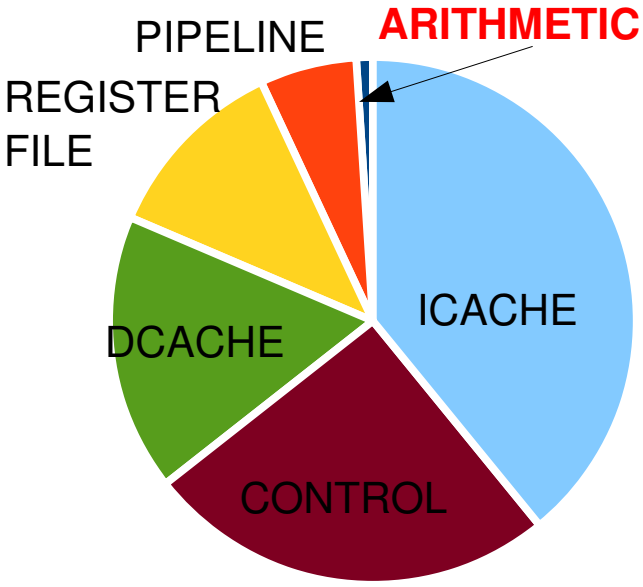


Peaceful coexistence between architectures...

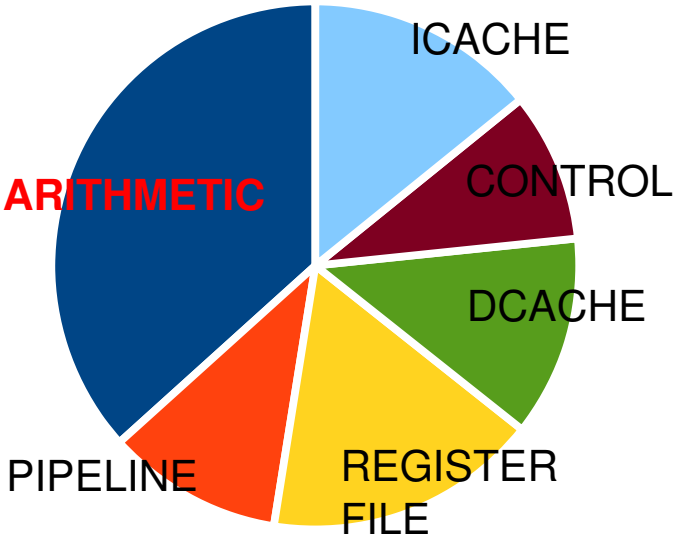
Energy Waste in Processors



GENERIC PROCESSOR



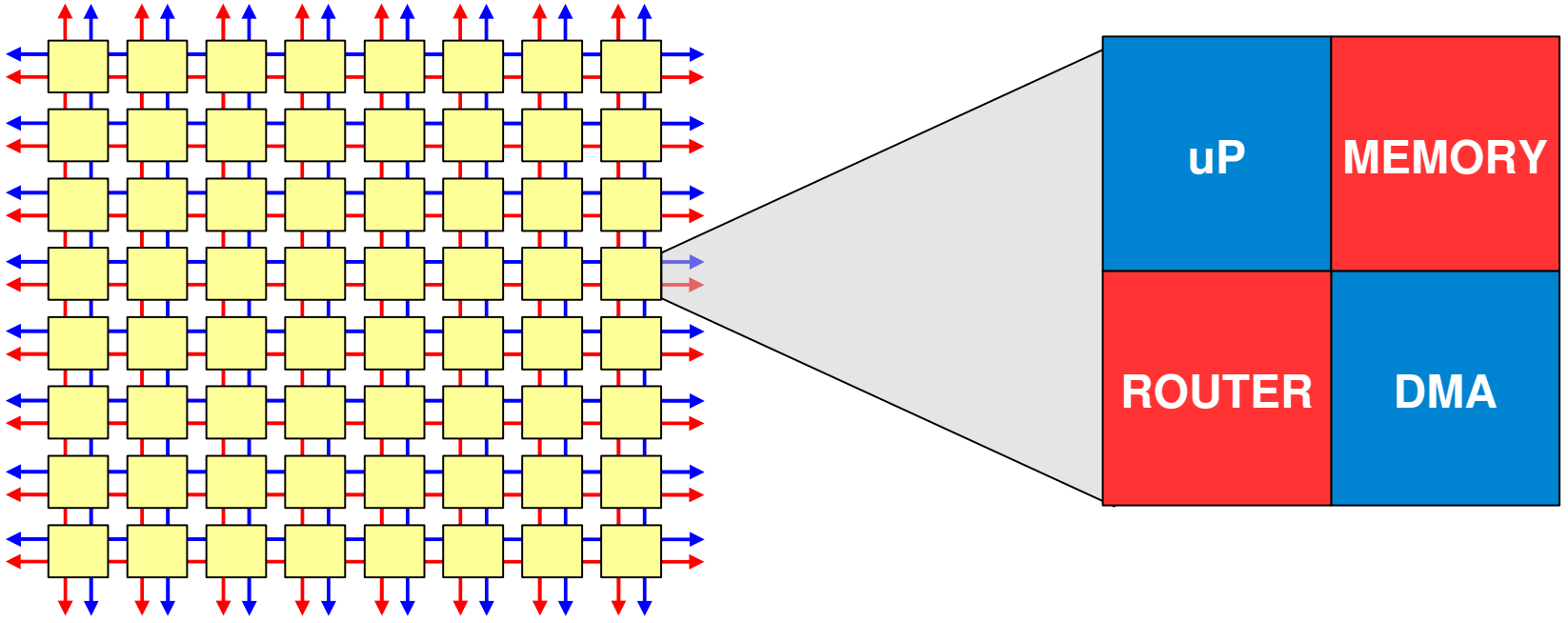
TYPICAL, 1% EFFICIENCY



FOCUSED, 37% EFFICIENCY

- Conclusion: The hardware-software energy efficiency gap can reduced from 100x to less than 3x with an appropriate architecture.

Adapteva's Vision for Soft ASICs



- ANSI C-programmable IEEE Floating Point Signal Processing
- 16 to 4096 independent cores

50 GFLOP/Watt @ 65nm
Real Performance