Improving Engineering Efficiency Through Tiled Hierarchical Flows

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The Future is Low Power

**2023 Super Computer Projection:**
- 10 GWatt System

**2023 Cellphone Projection:**
- Battery and processor gains will limit cell-phone feature sets

**2023 Data-center Projection:**
- Exponential growth of internet connectivity and cloud-computing will stall unless we reduce data-center power consumption.

**The Only Alternative:**
- Come up with a new architecture AND change the programming model
Adapteva Technology Introduction

- Mesh connected array of ANSI C-programmable processor cores
- 16 to 1024 independent dual issue microprocessors

- Autonomous low power NOC
- Flexible off-chip link protocol
- Floating point support

50 GFLOP/Watt Performance @ 65nm
Hierarchical vs Flat Design

**FLAT**

Advantages:
- Easy floor-planning
- Overall less work up front
- Smaller chip area (sometimes)
- Great for junk collection

Disadvantages:
- Tool capacity
- Slooooow iterations

**HIERARCHICAL**

Advantages:
- Deterministic timing closure
- Super fast iterations
- Scalable

Disadvantages:
- More work
- Tedious floor-planning
- Tool support issues
Adapteva Implementation Flow Introduction

- An all Magma tools flow from RTL to GDS
- Multi-million gate SOC with 64 SRAM macros
- 65nm triple Vt process technology
- Aggressive timing and power targets
- All off the shelf IP
- Hierarchical design flow
Adapteva Hierarchical Flow

- Abutted routing
- No global wires
- No synthesis at top level
- All macros hardened
Tiled Flow Lesson #1

Lesson: For symmetrical architectures tiled hierarchical flows work beautifully (hint...design with symmetry)

- One symmetrical core block:
  - Small and manageable blocks
  - The key was careful pin planning
  - High utilization
  - Aggressive timing constraints
  - Instantiated 16 times (but is really only limited by size of reticle)
  - Correct by design block to block communication
You can't scale without symmetry!!
Lesson: Know when to flatten design and when to use hierarchical design techniques

- Mistake:
  - Trying to connect everything by abutment
  - Hierarchical not ideal for asymmetric blocks with changing interfaces (i.e. IO)
  - Blocks with 50:1 aspect ration should be flattened!

- Next time:
  - A little flatter...
Tiled Flow Lesson #3

**Lesson:** *Know when to “tickle”*

**Tool limitations:**
- TALUS wouldn't connect our tieoffs correctly no matter how hard we tried
- Short point to point routing that wasn't on grid was a disaster.

**Solution:**
- Simple tcl scripts for point to point routing
Tiled Flow Lesson #4

Lesson: *Placing pins on multiple layers to force symmetry*

- **Problem**
  - Outer blocks needed to be flipped to talk to IO (asymmetric)
  - We didn’t want to create four different blocks!

- **Solution:**
  - Place duplicate ports on different metal layers and leave space between blocks at top level for connection
TFM/ATLAS Flow Overview

• Why use it?
  - Fast ramp-up time
  - Less risk
  - Good results with minimal effort
  - Very flexible

• Lessons Learned
  - Minimize code duplication by building code on top of TFM
  - Make sure it's easy to update flow

Example of header.tcl:

```tcl
set module  score
set verilogDefineList "-define CFG_RFAW=5"
set vlist    "core.v top.v ..."
```

Block Specific Files Called by variables.tcl

- header.tcl
- \${block}_constraints.tcl
- \${block}_floorplan.tcl
A few words on MOJAVE..

- Fantastic runtime and memory footprint. We had no problem verifying our multi-million gate ASIC on a 16GB quad core Opteron machine within hours.

- Direct read of CALIBRE runsets at 65nm worked fine, with the exception for antenna rules.

- Correctness of DRC and LVS runsets and verification engine verified through independent Calibre runs at the foundry.

- Fantastic support from Magma team.
Summary

• Tiled hierarchical design flows are here to stay!
  − Successful tapeout of multi-million gate SOC within 6 weeks of becoming a MAGMA customer
  − 2 weeks from new floor-plan to GDS-clean
  − 12 hour design cycle from RTL change to GDS clean
• The TALUS RTL to GDS flow offers the most complete implementation and most efficient flow this engineering has team has seen to date from any vendor.
• Don't buy the hype. With the right people and tools SOCs don't have to cost $75M.